AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A square root extraction circuit for ~~calculating~~ processing binary input data (0.a(1)) a(2) a(3) ... a(n)) using a square root extraction algorithm to output binary square root data (0.q(1) q(2) q(3) ... q(m)), said square root extraction algorithm including an algorithm for determining said square root data on the basis of said input data by only additions of square root partial data q(I) to q(m) in q(I) to q(m) order, said square root extraction circuit comprising:

first to *m*th digit calculating portions each including a plurality of adders connected in series to that carries are propagated therethrough, wherein respective ones of said adders which are connected in the last position in said first to *m*th digit calculating portions provide carry outputs serving as said square root partial data q(I) to q(m), respectively, in accordance with said square root extraction algorithm,

wherein ~~said plurality of adders include only a half adder and a full adder, and said full adder obtains only one bit of addition output and one bit of carry output based only on two bits of data input and one bit of carry input~~ said square root extraction circuit outputs said output binary square root data (0.q(1) q(2) q(3) ... q(m)) without using any controllable add/subtract cells.

Claims 2-12. (Canceled)

Claim 13. (New) The square root extraction circuit of claim 1, wherein said plurality of adders of each of first to *m*th digit calculating portions includes one half adder and at least one full adder.

Claim 14. (New) The square root extraction circuit of claim 1, wherein said plurality of adders of each of first to *m*th digit calculating portions include at least one full adder, said at least one full adder provides only one bit of additional output and one bit of carry output based only on two bits of data input and one bit of carry input.